IN THE ABSTRACT OF THE DISCLOSURE

Please amend the Abstract as follows:

In a computer system having a scalar processing unit and a vector processing unit, wherein the vector processing unit includes a vector dispatch unit, a system and method of executing a vector memory instruction having a scalar operand, decoupling operation of the scalar processing unit from that of the vector processing unit, the method comprising sending a vector instruction from the scalar processing unit to the vector dispatch unit, wherein sending includes marking the vector instruction as complete if the vector instruction is not a vector memory instruction and if the vector instruction does not require scalar operands, reading the a scalar operand, wherein reading includes transferring the scalar operand from the scalar processing unit to the vector dispatch unit, determining if the vector memory instruction is scalar committed and if the vector memory instruction is scalar committed, executing the vector memory operation predispatching the vector instruction within the vector dispatch unit if the vector instruction is scalar committed, dispatching the predispatched vector instruction if all required operands are ready, and executing the dispatched vector instruction as a function of the scalar operand.